R18

Code No: 156DF

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

B. Tech III Year II Semester Examinations, January/February - 2025

VLSI DESIGN

(Electronics and Communication Engineering)

Time: 3 Hours **Max. Marks: 75**

Note: i) Question paper consists of Part A, Part B.
ii) Part A is compulsory, which carries 25 marks. In Part A, Answer all questions.
iii) In Part B, Answer any one question from each unit. Each question carries 10 marks and may have a, b as sub questions.

PART – A

(25 Marks)

1.a)	What is a pass transistor?	[2]
b)	Mention the advantages of Bi-CMOS circuits.	[3]
c)	Mention the importance of scaling.	[2]
d)	Why spacing between n-diffusion to p-diffusion is large?	[3]
e)	Define Fan out.	[2]
f)	Mention the three sources of wiring capacitance.	[3]
g)	Mention the applications of counters.	[2]
h)	What are the limitations of SRAM?	[3]
i)	List out the chip level test techniques in VLSI.	[2]
j)	Mention any two differences between PLA and PAL.	[3]

PART – B

(50 Marks)

2.a) Explain the CMOS fabrication process with suitable diagrams.
b) Determine the pull-up to pull-down ratio for an NMOS inverter driven by another NMOS inverter. [5+5]

OR

3.a) Draw a simple BiCMOS inverter circuit diagram and explain its operation.
b) Explain the latch-up condition in CMOS Circuits and methods to eliminate it. [5+5]

4.a) Discuss in brief the effects and limitations of scaling on Substrate doping and interconnect and contact resistances.
b) Discuss the methodology to be followed in layout design. [5+5]

OR

5.a) Discuss in brief the effects and limitations of scaling on Logic levels and Supply voltage.
b) Mention different choices of layers to be considered in wiring a circuit. [5+5]

6.a) Draw the circuit of a logic gate using DCVS logic and explain the operation.
b) Explain the effect of wiring capacitance on the performance of VLSI circuits. [5+5]

OR

7.a) Draw the circuit of a logic gate using pseudo NMOS logic and explain the operation.
b) Write a brief note on Resistive interconnect delay. [5+5]

8.a) Explain the design and operation of a Multiplier.
b) Explain the design and operation of ROM. [5+5]

OR

9.a) Explain the design and operation of a SRAM.
b) Explain the design and operation of an ALU. [5+5]

10.a) Explain the design approach of a PAL.
b) What is testing? Explain the procedure to test single gates. [5+5]

OR

11.a) Explain the design approach of a FPGA.
b) Explain any one Chip level test technique. [5+5]

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